MZB-3 CPU MANUAL

Interak

PRODUCT INFORMATION
No. 101870

Incorporates M 101870 002

Document Ref: MZB-3/ (GE)

Issue:

Date: May 1981

(Replaces Issue 2, August 1980)

MZB-3 BUFFERED Z80 CPU 'KEMITRON' BOARD AND 'ISBUS' CONSIDERATIONS.

Document Price: £1.50

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Interak

ADDITIONAL NOTE TO THE FOURTH EDITION OF THE MZB-3 MANUAL 1982

MZB-3 Card at 4.0 MHz in an Interak 1 System

Throughout this Manual mention is made of the caution which must be employed when operating the MZB-3 card at 4.0 MHz.

However the recommendation now for Interak 1, and indeed the majority of all other uses, is to operate the card at 4.0 MHz, and to dispense entirely with any modifications to lower the frequency.

Operational experience has confirmed the designer's original contention that 100% satisfactory results can be obtained at this frequency. This is readily explained when it is realised that modern memory devices are vastly superior to the types which were generally available some years ago.

Therefore it is suggested that the inconvenience and reduced performance which is suffered when the card is modified for half-speed operation need no longer be tolerated, and thus the card should simply be assembled in the standard way for 4.0 MHz operation.

D.M.P. July 1982.

CONTENTS

1. Introduction

1.1 This 'Kemitron' board is the replacement for the earlier MZ1; although it has various advanced features, (which are directed to its ultimate use as the CPU board in a floppy disc system with large amounts of dynamic memory), it nevertheless is equally effective for use in quite small systems.

1.2 There is space for an EPROM of the 2708 type or 2516 (5V 2716) type. As the 2516 is the more modern device this is the type which is preferred. Extra components are required for the 2708 and although they would not normally be supplied, they are included in all the diagrams etc., for completeness.

2. ISBUS Compatibility

2.1 The International (3U high) size of card with its standard direct gold-plated 0.1" edge connector, is growing in popularity and there are a number of independent suppliers now actively engaged in designing new boards.

2.2 There are benefits which apply to suppliers and users alike, if a suitable bus standard can be defined, and for this reason Greenbank Electronics is actively promoting the ISBUS standard.

2.3 The ISBUS standard is still under discussion, but when complete it will define a total of 84 connections - 42 on the 'A' side, and 42 on the 'B' side of the board.

2.4 The more important signals of ISBUS are to be found on the 'A' side, and it is a major feature of ISBUS that a worth-while economic system can be built using only these lines, with the 'B' side being held in reserve only for those applications which require the highest performance regardless of cost. (The 'B' side is used to allow 16-bit microprocessors, extended address space past 64K, and multiprocessors on the same bus etc.)

2.5 The MZB-3 board has only 'A' side connectors, but these are largely ISBUS compatible. The circuit diagrams and drawings here have been written to help the user conform as closely as practical to the ISBUS standard.

2.6 Some small differences however will still remain, summarised as follows:-

Pin No.	Name	MZB-3	ISBUS
A21	NRST	TTL	Buffered Open Collector
A30	NENIN	Unused	Used
A31	NENOUT	Unused	Used
A32	NRFSH	Unbuffered	Buffered
A34	NWAIT	Unbuffered	Buffered

3. General Circuit Description

3.1 The circuit diagram (No. 101810) covers 6 sheets, pages 33-38 , and these represent convenient subdivisions for description.

3.2 Sheet 1 (Page 33), shows the crystal controlled clock oscillator. It has two outputs: Zø, which drives the CPU chip (IC10,Z80), and 'RCLK', which drives the bus via edge connector pin A33.

3.3 Sheet 2 (Page 34), is the diagram of the reset circuit. The output 'NRST' is used on the card and is also taken to the edge connector pin A21.

3.4 Sheet 3 (Page 35), shows the CPU chip itself, the power on jump circuit and 4K page decoder. (There is space on the board for an EPROM which can be located at any 4K boundary).

3.5 Sheet 4 (Page 36), shows the EPROM (IC 11). IC 2 is a dual flip-flop. The IC2a output 'PJUMP' is used for the 'POWER-ON-JUMP' feature, and the IC26 output is used to select the EPROM. Under software control IC2a can be reset, to remove the effect of the POWER-ON-JUMP, and IC2b can be reset to disable IC11, (so that some other memory devices, e.g. system dynamic RAM, can use the same addresses).

3.6 Arrangements like this are invaluable in 'Floppy Disc' systems: (All the programs in such a system are generally kept on the discs, the only firmware necessary being a 'bootstrap' PROM, in this case IC11, which is in circuit only long enough to get the system running, and which is then switched out).

3.7 Sheet 5 (Page 37) is the diagram of the buffers to the edge connector. The 8 bit data bus is bidirectional (IC17), and all other signals (address and control) are unidirectional (IC7, IC8, IC13).

4. Detailed Circuit Description

4.1 Clock Oscillator (Page 33)

4.1.1 IC9c and IC9a are used as amplifiers for a crystals controlled square wave oscillator. The frequency is set by X1 and frequencies commonly chosen by users are 2.0MHz, 2.5MHz, or 4MHz. IC9f is unused and is available for any special purpose the user may have.

4.1.2 The oscillator is buffered by IC9b and is taken via IC9e to 'Zø' (pin 6 on the CPU chip, IC10). The requirements of the CPU chip are fairly stringent regarding logic'1' level and the rise and fall times, particularly at 4MHz, and the circuit between pins 10 and 11 of IC9e forms an 'active pull up' to ensure the CPU chip clock specifications are met.

4.2 Reset Circuit (Page 34)

4.2.1 When power is first applied C6 and C5 are discharged holding the gate inputs (IC14d pin 12 and IC14a pin 2) at a logic '0'. This '0' on pin 2 of IC14a cause the output pin 3 to go to a '1' which is inverted back to a '0', so the NRST line is '0'; this resets the CPU (pin 26 of IC11).

4.2.2 R9 and R8 charge their respective capacitors and as C5 is smaller than C6 it goes to a '1' first. The Q output of the monostable (IC16 pin 6) is resting at a '1' by this time and thus both inputs of IC14a are '1'. The '0' output which results at pin 3 of IC14a is inverted by IC14b and NRST goes to a '1' hence the CPU begins to function.

4.2.3 The positive '0' to '1' transition on the NRST line is used as the clock pulse for pins 3 and 11 of the two type 'D' flip-flops contained in IC2. IC2 is shown on Page 36 , and the subsequent circuit operation is described below, Section 4.

4.2.4 IC15a will switch on in an indeterminate state, so it is possible that the first $\overline{M_1}$ cycle from the CPU ($\overline{ZM_1}$) will be inverted by IC14c and clock a '1' through from pin 2 of flip-flop IC15a to pin 5 of IC15a.

4.2.5 The resulting positive edge on pin 4 of monostable IC16 will trigger it and a short '0' pulse will be output at pin 6. This will pass through IC14a and IC14b to the NRST line temporarily producing the reset conditions again. In any event conditions will soon be stable and the CPU will begin operation continuously.

4.2.6 A short while after C5 goes to a '1', C6 will do the same. This '1' will be inverted by IC14d and the resulting '0' on pin 1 of IC15a will reset the Q output (pin 5 of IC15a) to a '0'. The negative edge from this Q output has no effect on the monostable IC16 since this is triggered only on positive edges at pin 4 of IC16.

4.2.7 The CPU chip will now run under program control until S1, the manual 'RESET' switch is operated. This will discharge C6 via R7. (R7 is included to limit the peak discharge current to about 24mA; without R7, higher currents would flow which could be damaging to C6 and S1).

4.2.8 With S1 closed pin 12 of IC14d is '0' and so pin 11 of IC14d is '1' and this removes the reset signal on pin 1 of IC15a a type 'D' flip-flop. The flip-flop outputs remain in the same state as they were (i.e. Q, pin 5, reset to '0' and Q pin 6 to '1') until a positive transition enters the clock pulse input pin 3 of IC15a.

4.2.9 Such a pulse is the result of a negative transition of $\overline{ZM1}$, which is inverted by IC14c. When it occurs the '1' on pin 2 of IC15a is clocked through to the output pin 5, which changes from '0' (reset) to '1'. Thus a positive edge is applied to the monostable input, pin 4 of IC16, and the monostable is triggered.

4.2.10 Pin 6 of IC16 is normally '1', and when the monostable is triggered pin 6 goes to '0' for a moment and then returns to its normal '1'. This '0' is inverted twice, by IC14a and IC14b, and so NRST, the system reset line, also goes to '0' for a moment.

4.2.11 No further NRST pulses occur until S1 is opened, C6 charged up and discharged again by a further closure of S1.

4.2.12 C7 and R10 set the period of the monostable to about 8 µS, which is more than sufficient to ensure the CPU resets properly, as the CPU reset line only has to remain active for about 3 or 4 clock cycles.

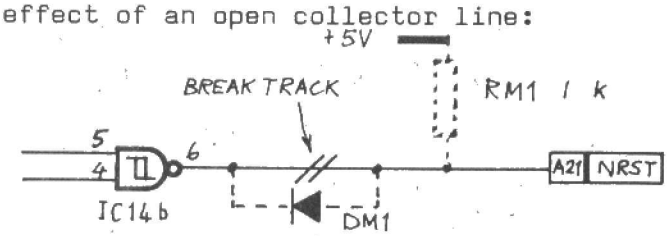
4.2.13 Even if the reset button S1 is held closed the CPU will not be permanently reset, and also the NRST pulse is synchronised by the falling edge of $\overline{ZM1}$.

4.2.14 The purposes of these measures is to ensure that data is preserved in any dynamic RAMs whose refresh is being controlled by the CPU. If the NRST line is held low for more than about 1ms, CPU refresh of dynamic RAM is suspended and the data is lost. The NRST pulse has to be synchronised by $\overline{ZM1}$ because it could otherwise possibly cause an aborted or shortened access of the dynamic RAM, (if NRST began in an inconvenient point in the CPU operating cycle), and destruction of data in the dynamic RAM.

4.2.15 If the system RAM is all static type not dynamic, or if the contents of the dynamic RAM is of no concern after Reset then this part of the circuit can be simplified: IC15, IC16 need not be fitted, and pin 12 of IC14d can be connected via a short insulated wire link to pin 1 or IC14a.

4.2.16 The reason for using Schmitt-trigger gates for IC14 is because the outputs of standard or Low-power-Schottky gates are not guaranteed to be 'clean' if the inputs are fed with slowly changing signals (such as charging capacitors C5 and C6). IC15b has no function in this circuit.

4.2.17 Note: According to the ISBUS specification the signal on pin 21 should be open collector (so that when it is '1' some other device (e.g. a simple switch) can reset the system remotely. It would be unduly pedantic to insist on strict adherence to the ISBUS specification on this point but the following circuit shows one expedient method to give the effect of an open collector line:



DM1 in this modification will have to be a germanium type, which has a much lower forward voltage drop than silicon types. Ideally an open collector buffer of some sort should be used but the above modification may be sufficient to get round the problem, if one exists.

4.3 CPU, Power on Jump, Page Decoder Circuit (Page 35)

4.3.1 This circuit shows the CPUchip (IC10) itself. Taking the pins largely in the order they are illustrated on the diagram the various functions are as follows:

4.3.2 Pin 6 'ZØ', is the clock input signal which is derived from the circuit already discussed in Section 4.1 above it regulates and defines the speed at which the CPU chip operates.

4.3.3 Pins 25, 16, 17 ($\overline{\text{BUSREQ}}$, $\overline{\text{INT}}$, $\overline{\text{NMI}}$) are all tied to a '1' by either R11 or R12. When they are '1' as here, they do not affect CPU operation. An external device would have to take the appropriate line to a '0' to obtain the desired response from the CPU, and the user is referred to the CPU chip data sheets for the description of this response. It is worth mentioning that pins 16 and 25 of IC10 would need to be separated if, as is likely invariably to be the case, individual control of each line was desired. For Mode 2 Interrupt the buffering needs alteration.

4.3.4 Pin 26, $\overline{\text{RESET}}$, is an input connected to the system NRST line whose action has already been discussed in section 4.2 above. A '0' on this line resets the CPU before operation under program control commences.

4.3.5.1 Pin 24 is the '$\overline{\text{WAIT}}$' input. When an external device wishes the CPU to wait it takes this line low. A typical example is a simple floppy disc control circuit which would have to ask the CPU to wait until the disc was in just the right position to receive its data. Another example is when the CPU is used with slow memory devices - a wait signal can be produced only by the slow memory address decoder or a crude method is for all memory accesses (fast or slow) to request that the CPU wait for a cycle or two.

4.3.5.2 In the absence of any such request R13 pulls pin 24 high so that the CPU is not asked to wait unnecessarily. The MZB3 board takes the NWAIT signal to position A30 on the edge connector, but 'ISBUS' board.(To do this cut the track between pads P20 and P21 on the upper (component) surface of the MZB3 board, and use a jumper wire J13 to connect P20 to P25 instead).

4.3.6 Pins 13, 10, 9, 7, 8, 12, 15, 14 are the 8 'tristate' data lines. They are bidirectional, and are sometimes inputs and sometimes outputs.

4.3.7 Pin 29 is the 0V power supply to the CPU chip.
Pin 11 is the +5V power supply to the CPU chip.

4.3.8 Pins 5, 4, 3, 2, 1, 40, 39, 38, 37, 36, 35, 34, 33, 32, 31, 30 are the 16 tristate address lines. They are all outputs. The design of the CPU-chip is such that the address bus is not guaranteed valid before the trailing edge of $\overline{\text{ZMREQ}}$ on an OP-Code Fetch. The CPU chip manufacturers suggest that a 4 bit latch be used on the top 4 address lines to avoid potentential difficulties in the interface to dynamic RAMs, and IC4, enabled by $\overline{\text{ZMREQ}}$ provides this function on this board.

4.3.9.1 Pin 28 of the CPU is the $\overline{\text{RFSH}}$ signal output. It goes to a '0' to indicate that the seven lower order bits of the address bus contain a refresh address for dynamic memories.

4.3.9.2 The signal if required is taken to edge connector pin A32 'NRFSH', via a jumper wire between circuit board pads P12 and P23.

4.3.10 Pin 23 on the CPU chip IC10 is another output: $\overline{\text{BUSAK}}$.
It goes to a '0' to indicate that the CPU busses are tristate. It is not likely to be used in this application, as the CPU busses are buffered from the edge connector independently.

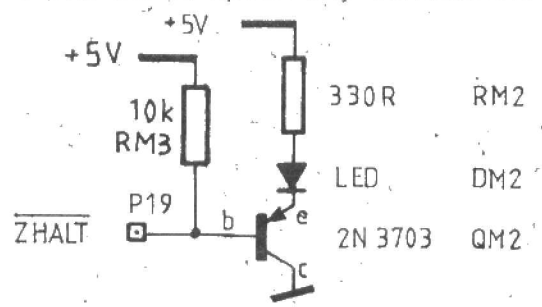
4.3.11 Pins 21 and 22 are the read and write control line outputs. They go low respectively to indicate that the CPU wants to read or write.

4.3.12 Pin 27 is the 'machine cycle one' output. It goes low to indicate the CPU is currently fetching an operation code (OP-code). Its main use here is for synchronisation purposes, e.g. for the reset circuitry described in section 4.2.

4.3.13 Pins 19 and 20 on IC10 are the '$\overline{\text{Memory Request}}$' and '$\overline{\text{I/O Request}}$' output signals which are buffered and used by the system. A '0' indicates that the address and data on the bus are associated with either the Memory or the Input/Output Ports, according to which line is '0'.

4.3.14.1 Pin 18 is a '$\overline{\text{HALT}}$' output which goes to a '0' to indicate that the CPU has just executed a 'HALT' instruction and is waiting for an interrupt input in order to continue. The signal can be used for various purposes, but if a visible indicator is required the following circuit can be used and built up in any convenient manner:

4.3.14.2



(QM2 is an emitter follower, which amplifies the current the CPU can sink into pin 18, to allow about 10mA (limited by RM2) to flow in L.E.D. DM2).

4.3.15.1 The PJUMP signal will be described in Section 4.4 but for the moment it can be taken that at 'power-on' it is at a '1'. The top 4 address lines, (which have been latched by $\overline{\text{ZMREQ}}$ in the manner already described) are the Q output pins 16, 15, 10, 9 or IC4 and a suitable combination of links, as listed in the 'Table of Jump Addresses' given on the diagram, will cause the 4 addresses JA15, JA14, JA13, JA12 to be set to any chosen 4K page. The method of operation is as follows:-

4.3.15.2 At 'power-on' the CPU issues an address on page 0 and so the 4 outputs of IC4 are all '0'. If the program in the system begins on page 0 then JA15, JA14, JA13

and JA12 should all be '0' and so Jumper links J2, J6, J4 and J8 should all be made. (In this case IC5 will be serving no purpose - the output of an 'OR' gate with '0' on both inputs is '0', and '1' if the inputs are '1').

4.3.15.3 However, if for some special purpose it is wished to locate the program on some other 4K page, then the links J1 to J8 can be rearranged to route the '1' from the PJUMP line into one or more of IC5's inputs and jam the address outputs to any chosen page. The table of address gives details of the specific jumper links to be inserted, but the basic principle is that if the output line is to be '0' the two 'OR' gate inputs are joined together to the appropriate IC4 Q output, and if a '1' is required, one of the 'OR' gate inputs is connected instead to the 'PJUMP' line.

4.3.15.4 (Of course, for a fixed page '0' it might be more convenient simply to remove IC5 and link pins 2-3, 12-11, 5-6, and 9-8 fitting none of links J1-J8).

4.3.15.5 Under software control PJUMP is usually returned to '0' at some stage and so the effect of the Jump address links is cancelled and JA15, 14, 13, 12 are then the same as the addresses A15, 14, 13, 12 issued by the CPU.

4.3.15.6 (The reason the power-on-jump feature is incorporated is to use the CPM floppy-disc operating system which requires RAM, not ROM, on page 0. In such a system all the programs are stored on magnetic discs, and transferred to the computer's RAM before they are run. This means there is no need for any ROM in the system, except for the tiny program which first loads the computer from disc.)

4.3.16.1 This ROM is called a 'Boot ROM' and is IC11 on this board. It obviously cannot reside on page 0 while loading RAM which is also at the same addresses, hence the necessity of a power-on-jump to some other clear address).

4.3.16.2 The remaining part of this circuit is the page decoder IC6. One of four links T_1 - T_4 one of four links T_5 - T_8 are inserted according to the table provided

on the diagram and these select the address of IC11, the on-board PROM. the top four address lines (J12, J13, J14, J15) are the inputs to IC6 and the selected page output SEL will go low when J12 - 15 correspond to the chosen page, as selected by links T_1 - T_8. Links T_1 - T_8 are single hole through ('thro') links which connect one side of the board to the other, so care should be taken to ensure no connection remains if a link is changed to another position.

4.3.16.3 The type of memory selected for the 'Boot PROM' IC11 is usually 1K or 2K and yet $\overline{SEL}$ covers an entire 4K page. Therefore no other device than IC11 can be located on the chosen page. This is generally of little consequence for a 'Boot PROM' as it remains in circuit only long enough to load the operating system into RAM from the floppy disc - it is then switched out of circuit leaving the whold SEL page clear for e.g. RAM.

4.4 The diagram on page 36 shows the 'Boot PROM' IC11 and some associated circuitry.

4.4.1 After the reset pulse NRST is over, the positive edge when it returns from '0' to '1' is used as a clock pulse for IC2a and IC2b (top left hand corner of the diagram. As the '0' inputs (pins 2 and 12) of IC2a and IC2b are both '1' this causes output Q (pin 5) 'PJUMP' to be '1' and output Q (pin 8) to be '0'. The 'PJUMP' output has already been discussed in section 4.3, and it is used to produce a chosen 'power-on-jump' to a chosen page.

4.4.2 The '0' output on pin 8 of IC2b is used to enable the on-board boot PROM, IC11. There are three inputs to the NOR-gate IC3a and at this stage IC3a, pin 2 is '0' because it is connected to pin 8 of IC2b. To read the boot PROM the CPU will have made $\overline{ZRD}$ a '0', and the issued address (modified by the power-on-jump circuit) will cause $\overline{SEL}$ also to be a '0'. This pin 1 of IC3a will be '0' because it is connected to $\overline{ZRD}$, pin 13 will be 0 because $\overline{SEL}$ is '0' and pin 2 is already '0'.

4.4.3 All '0's on the input to a NOR gate is the sole condition which causes its output, in this case pin 12 of IC3a to go to a '1'. Thus $\overline{\text{BUFFEN}}$ is '1' $\overline{\text{BUFFEN}}$ will be mentioned again in section 4.5 below but for the moment we shall simply say the $\overline{\text{BUFFEN}}$ = 1 is the condition which divorces the system data lines from the CPU data bus leaving them free to be controlled by the 'boot PROM' IC11.

4.4.4 The '1' on IC3a pin 12 is inverted to '0' by IC3b and this '0' is used to select IC11 via the chip select input pin 20 of IC11. Thus only the data from the on-board PROM IC11 at its power-on-jump address reaches the CPU.

4.4.5 When other addresses are isssued by the CPU $\overline{\text{SEL}}$ goes to a '1', and when the CPU is writing to memory ZRD is '1'. In these cases either or both pins 13 and 1 of IC3a are '1' and the putput pin 12 is '0'. This '0' on the $\overline{\text{BUFFEN}}$ line enables the data buffer so that the CPU has access to and from the system-data bus. The inverter-connected IC3b inverts the '0' to a '1' and so pin 20 of IC11 is high, effectively switching it out of the circuit.

4.4.6 As mentioned in Sections 3.5 and 3.6 , the main purpose of IC11 is to be a 'boot PROM' in a floppy disc system, and once it has completed its brief but all important task, the power-on-jump line PJUMP should be returned to '0' and the boot PROM should be switched permanently out. This is achieved in two stages under software control as follows:

4.4.7 Firstly a 'READ FROM OUTPUT PORT FF' CPU instruction is executed. This causes the eight address lines ZA0-ZA7 to go to all '1's (since 'FF' = all '1's), $\overline{\text{ZI/O}}$ goes to a '0' to indicate an I/O request, and $\overline{\text{ZRD}}$ goes to low for a read. The eight '1's on the inputs of IC12 are 'NANDED' to make output pin 8 of IC12 a '0'. The two '0's on pins 1 and 2 or IC1a leave output pin 3 as a '0' and the two '0' on pins 9 and 10 of IC1c result in a '0' on pin 1 of IC2a which resets it to '0', thus making PJUMP '0' and removing the power-on jump.

4.4.8 Secondly a 'WRITE TO OUTPUT PORT FF' CPU instruction is executed. As in the previous paragraph, output pin 3 of IC1a is '0' and therefore so is pin 12 of IC1d. $\overline{ZWR}$ is '0' for a write and this is connected to pin 13, the other input of IC1d. The output pin 11 of IC1d is '0' and thus IC2b gets reset: Q, pin 8 of IC2b, is one of the inputs of IC3a, and is now fixed at '1'. A '1' on any input of a 'NOR-gate'(IC3a) causes an output '0' regardless of the state of the other inputs, $\overline{SEL}$ pin 13 and $\overline{ZRD}$ pin 1.

4.4.9 Henceforth PJUMP is '0', removing the power-on-jump address, $\overline{BUFFEN}$ is '0' permanently enabling the 8-bit system data buffer, and $\overline{CS}$ pin 20 of IC11 is '1' permanently deselecting it.

4.4.10 IC can be either a 2516 or 2708 type of EPROM. If cost can be disregarded the best device is the 2516, since it is easy to program and requires only a single 5V supply. Although the 2708 device is cheaper it has the disadvantage that it needs additional supply voltages +12V, and -5V. Although +12V is a standard 'ISBUS' power rail, -5V is not, and so -5V has to be derived from the -12V standard 'ISBUS' power rail. Fortunately a simple series connected 6.8V Zener diode will drop approximatley 7 volts and the -5V supply for the 2708 is quite simply obtained from the standard -12V.

4.4.11 The appropriate changes are given in the notes at the top right hand side of the diagram on page 36. It is vital to get these connections absolutely correct as a wrong connection in this area is almost certain to cause damage.

4.4.12 (The 2708 type of EPROM consumes about 40 mA and so the dissipation in the 6.8V Zener is fairly large at about 280mW. This is why the technique is not used where several 2708s are involved, and a proper -12V to -5V regulator is used instead).

4.4.13 Of course if the user wishes to deviate from the ISBUS standards, it is perfectly possible to supply -5V to the edge connector pins A38 and A39, in which case no track cutting or Zener Diode is necessary.

4.4.14 IC1b and IC3c are not used in this circuit and so are available for any special purposes the user may have.

4.5.1 The circuit of the buffers (page 37) needs hardly any explanation. ICs 7, 8, 13 are standard non-inverting buffers which buffer the named signals. They are permanently enabled by having their 'Enable' pins $\overline{E1}$ and $\overline{E2}$ connected to '0'. Because both enable pins are at '0' it is possible to substitute different devices in a case of supply difficulty. The alternative types are named on this diagram.

4.5.2 IC17 is an octal bidirectional transceiver. Pin 19 is the single enable input E, connected to the $\overline{BUFFEN}$ line which has already been discussed in section 4.4.

4.5.3 When $\overline{BUFFEN}$ is '1' both sides of IC17 are tristate, but when it is '0' one or other of the two 8-bit sides is connected to the other side. The direction is controlled by the $\overline{ZRD}$ signal, connected to pin 1 of IC17.

4.5.4 When $\overline{ZRD}$ is '0' (i.e. the CPU is wishing to 'read' the data on the system data bus DB0 - DB7), the direction is from the 'B' side to the 'A' side of IC17, that is from DB0-7 to ZD0-7. When the CPU is 'writing' to the system data bus $\overline{ZRD}$ is '1', and in this case the direction is from the 'A' side to the 'B' side i.e. from ZD0-7 to DB0-7.

4.5.5 For special applications it may be desired to 'tristate' the bus and effectively isolate the board from the system. This is simply achieved in ICs 7, 8, 13 by taking their respective 'Enable' lines to a '1'. IC17 presents more of a problem: either pin 19 must be forced to an unconditional '1' or the direction must be permanently reversed by presenting an unconditional '0' to pin 1. It is likely some of the spare gates e.g. IC1b, IC3c, IC9f can be used to advantage to achieve this.

4.6 Power Supply and Decoupling Capacitors (Page 38)

4.6.1 This is the remaining section of the circuit diagram. It is mainly for reference purposes, for example when

testing or fault finding. Some of the symbols used on the diagrams are explained and the various power supply connections and decoupling capacitors are identified.

4.6.2 Although the power supply connections are largely irrelevant to logic diagrams, as are the decoupling capacitors and therefore often left off such diagrams, they nevertheless represent invaluable information when fault finding.

4.6.3 Both options for IC11 have been listed, and both ends of the capacitors (in common with all the resistors and capacitors on all the diagrams) have been numbered 1 and 2, to help during testing.

4.6.4.1 Except for R1 (top left hand corner of diagram on page 36), all TTL '1's have been connected directly to the +5V rail, without a limiting resistor.

4.6.4.2 There is a school of thought that says a limiting resistor should be included when connecting a TTL, or LSTTL etc., input to the +5V line. TTL inputs are connected to the emitter of a base-emitter junction which breaks down at about 9 volts, the action being similar to a Zener diode, and the resistor is included to keep the current down to a few mA to prevent permanent damage. See correction below.*

4.6.4.3 Kemitron's argument in leaving this component out is that the +5V line should never rise to +9V in any circumstances, and with modern crowbar protected power supplies there is a lot of truth in this statement. Certainly actual operating experience confirms that damage due to this cause is unlikely. We have heard of an isolated case of unexplained damage to a computer, but this was reported to have taken place during a thunderstorm, and it is debatable whether any measures can be taken to provide protection against lightining strikes! See correction below.*

5. Assembly

5.1.1 The Assembly Drawing (No. 101930) is to be found on Page 39, and the Parts List (No. 101840) is on Page 40.

*Correction 21.5.81: Closer examination reveals that the devices referred to are types 74LS74, 74LS122, and 74LS132 - none of these types have the vulnerable base-emitter junction described, so there is no cause for alarm!

5.1.2 The components have been numbered on the Assembly Drawing (No. 101830, page 39), in ascending numerical order. Viewing the board in the orientation that it will have in the computer (i.e. 'landscape' not 'portrait' position), numbering begins at the top left hand corner and proceeds in horizontal lines. For example 'IC4' is the fourth IC along,'IC6' is the sixth and so on.

5.1.5 The Parts List has the components listed in two ways. Firstly by the circuit reference number R1, R2, R3 etc., which gives the component value if the reference number is known, and secondly by the component value 22R, 220R, 1K etc., which gives the circuit reference numbers with that value.

5.1.6 This latter feature is quite helpful during assembly as for example, all 7 10K resistors can be collected together and installed at the same time, rather than in 7 individual operations. It is also helpful when collecting together or checking a 'kit' of parts.

5.1.7 There are numerous 'thro' wire links to be fitted, but these are not marked on the diagram because they are easier to see on the board itself. Short lengths of wire (e.g. resistor lead off-cuts) can be used, or purpose made 'thro' pins.. Do not fit the numbered links T1 to T10 until you understand their purpose - they will not all be needed.

5.1.8 It is worth mentioning that it would cost more to have a 'thro' hole plated board than it would cost to pay someone (e.g. Greenbank Electronics) to solder in the 'thro' links for you. So if there is anyone who is willing to pay the extra to avoid soldering his own 'thro' links remember..... it can be arranged!

5.1.9 It is assumed that the user will have sufficient experience to be able to identify the various components and to install them properly with due regard to polarity where this matters. Please contact us if this assumption is incorrect in your particular case, as it is possible to make some very expensive mistakes.

5.2 We would imagine however that even the experienced user would appreciate a brief list of some of the main points where an individual decision must be taken, which will affect construction:

5.2 (continued)

(i) Decide whether a card front or simple card handle is to be fitted and drill the board accordingly.

(ii) If the polarising slot (position A37, B37 on the edge connector) is required this should be cut at an early stage of construction, if not already present.

(iii) Protect the gold plating at all times against damage due to finger marks, solder, and scratches.

(iv) If it is wished to conform to the ISBUS allocations for NWAIT cut the copper track on the upper (component) side of the board between positions P20 and P21. Use an insulated wire jumper (J13) to connect P20 to P25 and so transfer the NWAIT line to edge connector A34.

(v) If IC11 is to be a 2708 instead of the (preferred) 2516, then -5V should be used on edge connector pins A38, A39. Alternatively, as the 'ISBUS' standard allocates -12V to A38, A39, then a modification is required if IC11 is a 2708: Cut the track on the under (non-component) side of the board between P14 and P15 and insert D1 (carefully, as the board designer has provided no space for this modification) on the component side between P14 and P15, cathode to P14.

(vi) If IC11 is a type 2516 then C11, C12, and D1 need not be fitted, and it is important to isolate the +12V and -12V edge connector voltages (A35, 36 and A38, 39) from the rest of the board. A convenient method is to omit T9 and T10, the two through board links which carry +12V and -12V, but there is no substitute for a physically cut track to give the maximum confidence that the voltage rails have been properly isolated.

(vii) If IC11 is a type 2516 then J9 and J10 both marked '6' should be fitted. It is essential to leave these out if IC11 is a type 2708.

5.2 (continued)

(viii) Note that J9 is positioned beneath IC10, and will require fitting before the IC, also some types of IC socket will be unsuitable.

(ix) Note also that Kemitron, the board designers, have positioned C9 beneath IC10. If the capacitor is too large to fit as intended, it should be fitted on the underside of the board or omitted altogether, we have heard of no problems omitting it.

(x) J11 and J12 can be left off NRFSH and RCLK are not required on the system bus. For 'ISBUS' compatibility J11 and J12 should be fitted.

(xi) When inserting through links note that only one of T1-4 and one of T5-8 should be fitted, also note that only half the Jumper links J1-8 are required. Consult the tables at the right hand side of the diagram on page 35 and the Section 4.3 for details.

6. Fault Finding

6.1 Most faults are due to poorly soldered joints, open or short circuits or misplaced components, and can be located by an extremely searching visual inspection.

6.2 Regrettably the techniques of finding more complex faults depend so much on what equipment, facilities and experience is available, that it will not be attempted to give more guidance here.

6.3 If you are not able to find a fault yourself then please consult us for details of our after sales service. (For obvious reasons, this service is limited only to those customers who have purchased the board from GREENBANK ELECTRONICS).

7. Applications

7.1 The primary application of the MZB-3 card is the CPU card in a large ISBUS system with up to 64K of Dynamic RAM, supporting the CPM disc operating system with several 5" or 8" floppy disc drives.

The full buffering on the address and data lines means that expansion can proceed without any need for concern for the loading effect as more and more memory or I/O cards are added.

The on-board 'boot-PROM' is specifically arranged for the requirements of a floppy disc system, and therefore should be seriously considered even if the addition of floppy discs is not envisaged in your own system at present. It is possible tha a CPU card without these features would have to be discarded entirely when floppy discs are added.
Hence the main application of the MZB-3 card is as the CPU card in an existing system which will eventually support floppy discs at some future date.

7.2 If the expense of floppy discs cannot be justified at present the same techniques can be used by storing all the programs on tape. As with the floppy disc system, there is little or no ROM, and RAM begins from location zero. The on board 'boot PROM' in this case will be used to load the program data from tape and then will be switched out of the circuit.

7.3 The recommended type 2516 EPROM for IC11 is 2K x 8 in length, easy to program, and needs only a single 5V power supply. A simple program such as Tiny BASIC could be used as IC11 as a conventional piece of piece of firmware starting at zero, without any of the power-on-jump boot PROM features being used. In this way the expense of separate ROM card could be saved in the early stages to give a very cheap system, without compromising in any way the potential for full expansion later as funds permitted.

7.4 The same remarks as in 7.3 above apply if the chosen firmware was a machine - code monitor program.

7.5.1 Although no work has been carried out on this subject it is likely that the board could be modified to use a 2532 instead of a 2516 EPROM, for IC11.

7.5.2 If this were done it means that the board could carry up to 4K of on-board firmware, which would make it suitable for use in a very small two-card computer for dedicated control or other industrial applications. (The second board, which is not a proposed design at present, would have some RAM and some I/O - at the mininimum this could

be a single RAM-I/O chip e.g. type INS 8154, but possibly the Z80 PIO would be a more appealing I/O chip).

7.6 The reader will be aware of the limited expansion capabilities of some of the various cheap computers which have been designed with low cost as their primary goal. The MZB-3 card has been designed with performance as its first priority and this is why for example the edge connector is gold-plated and the board is extensively buffered.

7.7 There are two applications where cost is very important. One is in a minimum system where the user is not experienced enough to appreciate the merits of a flexible, expandable design, and he has to make his decisions on the basis of price alone. The other application is, as described in section 7.5 above, where the board is part of a small dedicated system, probably selling in large numbers so every penny saved counts.

7.8 For these applications it is worth mentioning that several of the features of the board can be removed, to reduce the cost. No work has been done yet on the feasability of the following suggestions but they might be of interest if cost is an important factor:

7.9 If the power on jump and PROM disable facility is not needed and partial address decoding is permitted ICs 1, 3, 4, 5, 6, 12 are largely superfluous and with little modification can probably be removed.

7.10 If also the system is small the 4 buffer IC's 7, 8, 13, 17 can be removed and replaced by links straight to the edge connector bus.

7.11 If there is no dynamic RAM, or if data can be lost after RESET, then IC15, 16 C7 and R10 can be removed and replaced by appropriate links.

7.12 If the CPU can be run at a lower speed there is less need for an active pull up and C3, Q1, R4 and R6 can be removed and R5 end 2 connected as a passive pull up to IC9e pin 10, see diagram Page 33.

7.13 Naturally, the suggestions given for cost savings are not recommended whole-heartedly, but they are quoted to show that the MZB-3 board is as suitable for simple cost sensitive applications as it is for large (and expensive) floppy disc based computer applications.

7.14 It is not always true that 'what'll do a lot'll do a little' but in this case it is clear that the MZB-3 board should not automatically be dismissed as being too good for a particular application - it can be made as bad as the worst computer you know if you try hard enough!

7.15 To use the MZB-3 board as a plain CPU board without the power-on jump, fit links J2, J4, J6, J8 diagram page 35; this leaves the top four addresses unaffected, i.e. the first instruction is fetched from address '0'.

7.16 It is possible to have two pieces of firmware in a system at the same address, if one is installed as IC11 on the MZB-3 board and the other is elsewhere. At switch-on or on resetting the computer, IC11 will appear at the chosen address, but it can be switched out letting the other firmware take over (or RAM), by outputting any data to Port FF (e.g. the ZYMON 1 command 'P FF dd'). Erratic results should of course be expected if the CPU is actually executing code in IC11 when it is switched out!

7.17 If all of the firmware is to be mounted off the board, i.e IC11 is not to be fitted then the output buffer IC17 must have pin 19 '$\overline{\text{BUFFEN}}$' permanently low (Drg. No. 101810 sheet 5 on page 37). '$\overline{\text{BUFFEN}}$' is the output pin 12 of IC3a (see Drg. No. 101810 sheet 4 on page 36). Pin 12 of IC3a will be always low if input pin 13 '$\overline{\text{SEL}}$' is always high. If reference is now made to Drg. No. 101810 sheet 3 on page 35, it will be seen that '$\overline{\text{SEL}}$' is one of the outputs of IC6b, taken via one of the through links T1,T2,T3,T4. Thus, to make '$\overline{\text{BUFFEN}}$' low, '$\overline{\text{SEL}}$' must be kept high; this is fairly easy to achieve by removing IC6 altogether or the links T1,2,3,4 - '$\overline{\text{SEL}}$' will then be open-circuit and will float high, having the desired result, but to do the job properly '$\overline{\text{SEL}}$' should not be left open but should instead be connected to +5V.

Appendix 1: Use of 4.0MHz CPU Clock Frequency

8.1 Factors Influencing Choice of Crystal (Clock) Frequency.

8.1.1 Throughout this document the CPU chosen has been the higher speed version 4.0 MHz, as opposed to the 2.5 MHz version. This decision was based on economic grounds: At the time of writing a quartz crystal of 2.0 or 2.5 MHz is about £1.00 dearer than the 4.0 MHz type, and the 2.5 MHz CPU is only about £1.00 cheaper than the 4.0 MHz version.

8.1.2 In other words, provided the quartz crystal price is considered as well, there is little or no difference in total cost whatever speed CPU is chosen, and so the choice of the higher performance CPU represents the best value for money.

8.1.3 As will be discussed in the various Sections which follow, increased speed can often be more trouble than it is worth, and accordingly a method of modifying the MZB-3 circuit is described. The modification requires no extra parts, yet provides the option of 2.0 MHz or 4.0 MHz operation. It is fairly easy to make a fast circuit run slowly ('downgrade' to 2.0 MHz), but difficult or impossible to do the reverse, and this is another vindication of the decision to specify the 4.0 MHz CPU as standard.

8.2 Access Time.

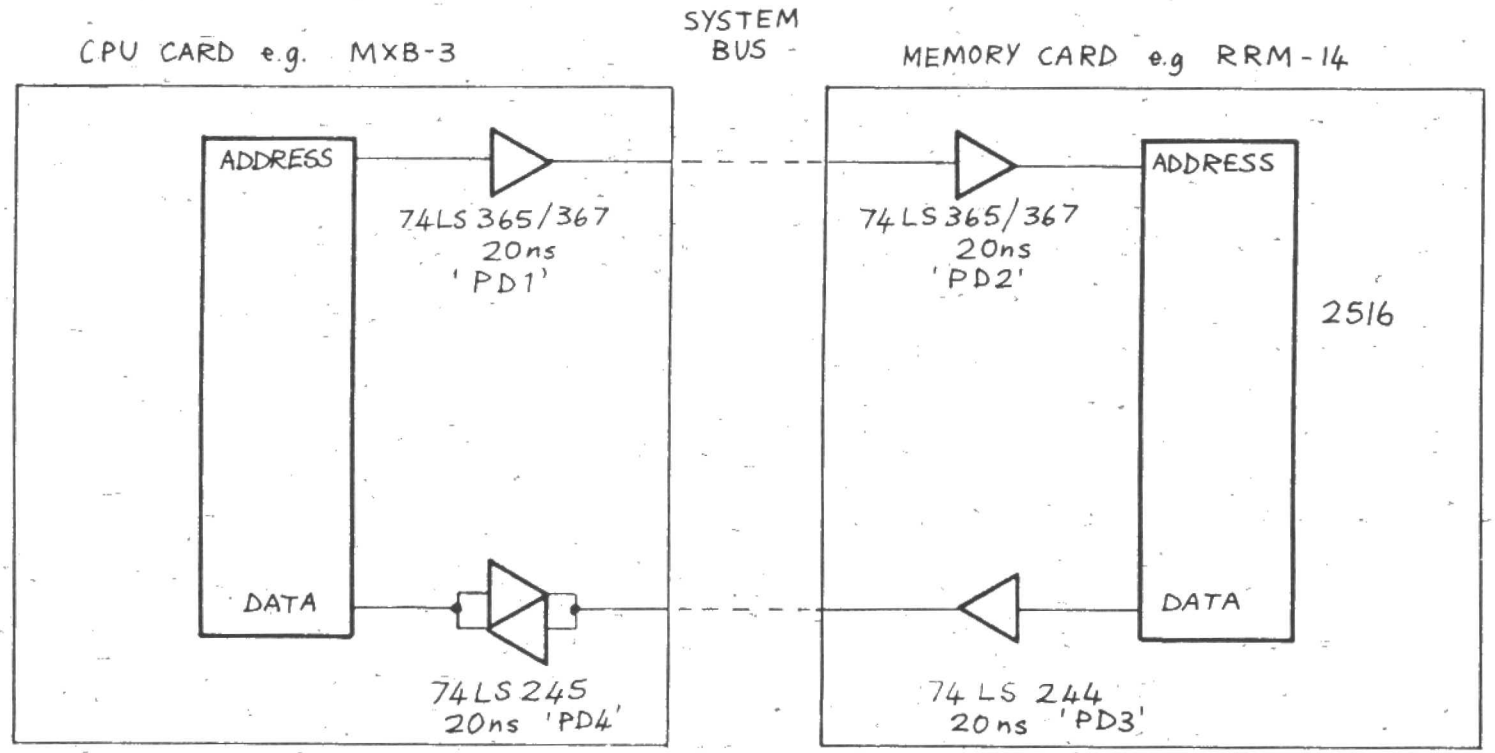
8.2.1 The main difficulty with 4.0 MHz operation is 'Access Time' restrictions. (The Access Time is the time it takes for a memory device to produce its correct data once its address lines are correct). Diagram No. 101871 'MZB-3 Buffer Delays in a Typical System' (Page 24), shows how buffer delays mount up. In the system taken as the example, up to 80ns can be lost. Assuming that it is a 2516 which is being addressed, and further assuming that it can only guarantee valid data 450 ns later, then the CPU must be prepared to wait 450 + 80 = 530 ns before it can expect valid data on its data lines.

8.2.2 The problem is aggravated when dynamic memories are being used. The address circuits generally used only present the address to the RAM after NMREQ has gone low, which is later than the time the addresses are first valid, the case considered in Section 8.2.1 above.

8.2.3 As the CPU speed increases, so the rate at which it expects data increases, and shorter and shorter memory access times result.

8.2.4 In order to ensure that the 'worst case' specifications are met, as far as is practical, it is necessary to study all of the various device data sheets extensively. Simply building a system and testing it to show it works is not good enough, and can give rise to vague complaints such as 'when I use this instruction the program sometimes fails', or 'After a few hours' use, the memory begins to fade, but only in warm weather' etc. Problems with dynamic RAMs used to be so common that they were given the name 'Memory Plague' by some suppliers.

DRG. NO. 101871	1 OF 1



TOTAL BUFFER DELAY 'TB' = 'PD1' + 'PD2' + 'PD3' + 'PD4'
= 80ns

NOTE 1: DELAYS SHOWN ARE DATA SHEET MAXIMA, TYPICAL DEVICES WILL EXHIBIT LESS DELAY.

NOTE 2: DIFFERENT 'LS MANUFACTURERS SHOW DIFFERENT MAXIMA FOR THE SAME DEVICE SO DELAYS SHOWN ARE BASED ON FIGURES ROUNDED TO THE NEAREST 5 NS.

		MOD 002: D.M.P. 4.8.80	001 DRAWN: D.M.P. 21.7.80	GREENBANK ELECTRONICS	
				MZB-3 BUFFER DELAYS IN A TYPICAL SYSTEM	
				DRG. NO. 101871	1 OF 1

8.2.5 Some very well-known names are responsible for 'suspect' designs of this nature - you can be sure something is wrong if it is necessary to swop memory i.c.s around on the board to make it work, or to use only a particular make of buffer, with a given batch code etc.

8.2.6 It will be shown during the course of these notes that correct operation cannot be guaranteed with a 4.0 MHz CPU clock frequency, for 450ns static RAMs and EPROMs. Even the fastest dynamic RAM generally available (type 4116-2, 150ns) cannot be used at this frequency, as it requires a NRAS precharge time of at least 100ns, and the CPU can only provide 95ns when it is running at 4.0 MHz. However, actual operating experience entirely contradicts this:

8.2.7 It has been found in practice that this board, and its companion dynamic RAM card MXD-2, operate satisfactorily at 4.0 MHz, but it should be stressed that this is due to the good nature of the chip manufacturers, who almost invariably supply chips which are vastly superior to their 'worst case' data sheet limits.

8.2.8 The MZB-3 Memory Access Timing Diagram is to be found on page 26. The full details are given in the appropriate manufacturers data sheets, and only the salient features are reproduced here. The timing illustrated is the most stringent of all the Z80/MK3880 cycles: the '$\overline{M1}$' or 'Op-Code Fetch' cycle, which is shorter than the subsequent memory accesses.

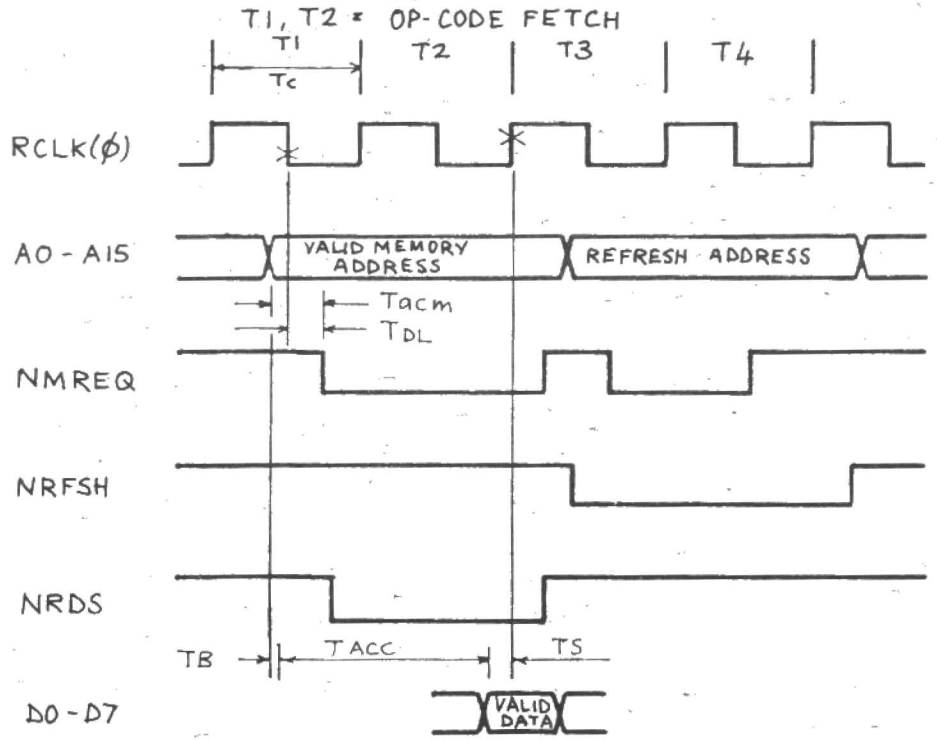
8.2.9 The table to the right of the diagram lists the relevant parameters at the three clock frequencies, and concludes that the access time for the memories required to work with the CPU at 2.0 MHz, 2.5 MHz, and 4.0 MHz are 725ns, 525ns, and 275ns, respectively. Thus at 2.0 and 2.5 MHz, the standard 450ns 2114s, 2516s etc. are suitable, but at 4.0 MHz the requirement shrinks to 275ns, and prohibits the use of the common memory devices.

8.2.10 The on-board 'boot PROM' is mounted on the MZB-3 board before the buffers, and is therefore not subject to the buffer delays. This means that the figure of 80ns for T_B used on Drawing No. 101872 can be reduced to zero. Thus the maximum access times for IC11 with the CPU clock at 2.0, 2.5, and 4.0 MHz, are 805ns, 605ns, and 355ns respectively. The main conclusion which must be drawn is that even for the on-board PROM 4.0 MHz is too fast if a standard 450ns type is used.

8.2.11 Thus at 4.0 MHz it is likely (depending on actual system delays), that a 350ns component is needed for IC11, and 250ns for off-board memories.

8.2.12 To permit the use of standard 450ns memories, one possibility is to add 'WAIT' states to the circuit. At 4.0 MHz each WAIT state added extends the access time by 250ns, so a single WAIT state (for all accesses, not just $\overline{M1}$) will be sufficient.

DRG. NO. 101872	1 OF 1



OP-CODE FETCH (M1) CYCLE, AS ILLUSTRATED

		← Z80 →		← Z80A		
CLOCK FREQUENCY	ϕ	2·0	2·5	4·0	MHz	NOTES
CLOCK PERIOD	Tc	500	400	250	ns	
NMREQ DELAY	TDL	100	100	75	ns	
STABLE ADDRESS	Tacm	205	155	90	ns	
BUFFER DELAY	TB	80	80	80	ns	1
SET UP TIME	Ts	50	50	35	ns	
CALCULATED ACCESS TIME	TAcc	725	525	275	ns	2

TIMES FOR NON-M1 MEMORY READ (NOT ILLUSTRTED)

CALCULATED ACCESS TIME	TACC2	915	715	375	ns	3

NOTE 1: SEE DRAWING NO. 101871 'BUFFER DELAYS IN A TYPICAL SYSTEM', WHERE TB IS CALCULATED.

NOTE 2: $TACC = 3/2\ TC - TDL + Tacm - TB - Ts$

NOTE 3: TACC2 : AS FOR TACC BUT USING $4/2$ TC (AND DIFFERENT TS, OTHER PARAMETERS AS SHOWN IN TABLE).

NOTE 4: ACCESS TIMES FOR DYNAMIC RAMS ARE MUCH REDUCED, SINCE TIMING BEGINS GENERALLY MUCH LATER (FROM MREQ 'L').

		MOD 002 : DMP. 4.8.80	001 DRAWN: DMP 21.7.80	GREENBANK ELECTRONICS
				MZB-3 MEMORY ACCESS TIMING
				DRG. NO. 101872 | 1 OF 1

8.2.13 As the WAIT states slow the CPU down they tend to act so as to reduce some of the benefit of operating at 4.0 MHz. (There is usually a net benefit however, as when the CPU has finished waiting it can then resume operation at top speed; a slower CPU is slower all the time).

8.2.14 The ideal arrangement for entering WAIT states is for the (slow) memory to pull the A34 (NWAIT) bus line low for as long as it needs, timing either by a monostable, or some method of counting clock pulses.

8.2.15 As none of the 'Kemitron' boards provide this facility, on the grounds of avoiding undue complication, no further details are given here. Extra information regarding WAIT states is given in the appropriate data sheets and books.

8.2.16 IC11 on the MZB-3 board is also affected, so if this i.c. is fitted then extra WAIT states must be provided for this component also.

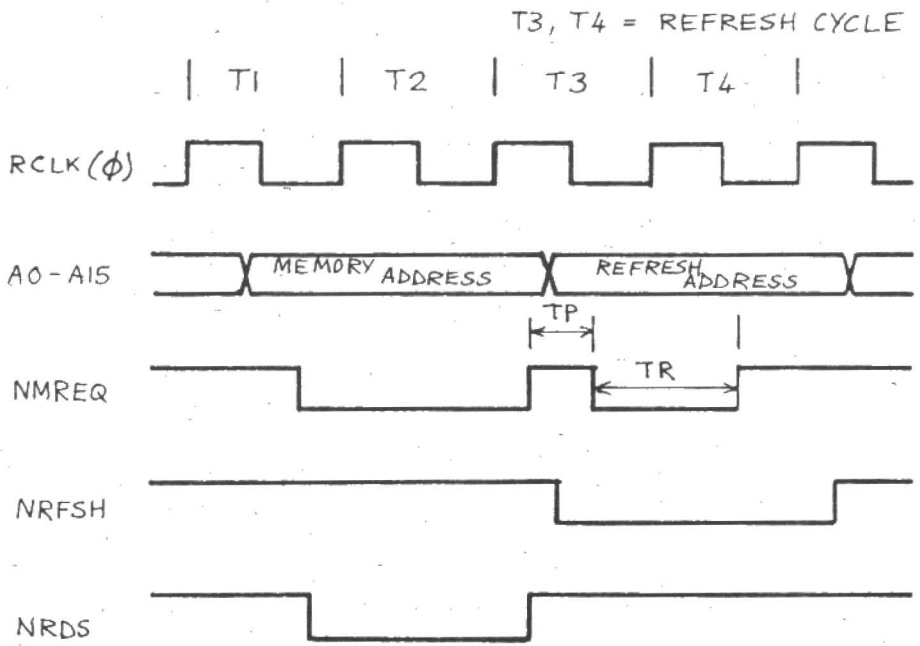
8.3 Dynamic RAMs.

8.3.1 Dynamic RAMs offer the great benefits of very low cost, and reduced power consumption. They are however a little more difficult to understand, and the task of circuit design is more complicated.

8.3.2 The user should be careful not to make the mistake of thinking that for example a 250ns dynamic RAM will give any benefit over a 450ns static RAM, when considering access timing. There are various parameters, such as address multiplexer delays, precharge times, and cycle times, for dynamic RAMs which must also be taken into account.

8.3.4 With a 4.0 MHz CPU the access time depends on the various buffer, decoding , etc. delays, and it is likely that the 4116-2 (150ns) type will be needed, which is disproportionately expensive, due to the high popularity of the 'normal' 4116-4 (250ns) type, which keeps its price down.

8.3.5 The main problem with the use of dynamic RAMs is not directly related to the question of access times, but occurs during the 'refresh cycle'. See Drawing No. 101873 'MZB-3 Refresh Cycle Timing', on page 28.



NRAS PRECHARGE TIMING FOR DYNAMIC RAMS

CLOCK FREQUENCY	φ	Z80 2·0	Z80 2·5	Z80A 4·0	MHz	NOTES
NRAS PRECHARGE TIME AVAILABLE	TP	210	160	95	ns	
PRECHARGE TIME REQUIRED 4116-2	TP	— 100 —			ns	1
— " — 4116-3	TP	— 120 —			ns	1
— " — 4116-4	TP	— 150 —			ns	1

TNRAS TIMING FOR DYNAMIC RAMS

CLOCK FREQUENCY	φ	Z80 2·0	Z80 2·5	Z80A 4·0	MHz	NOTES
TNRAS AVAILABLE	TR	460	360	220	ns	
TNRAS REQUIRED 4116-2	TR	— 150 —			ns	2
— " — 4116-3	TR	— 200 —			ns	2
— " — 4116-4	TR	— 250 —			ns	3

NOTE 1: AT A CLOCK FREQUENCY OF 4·0 MHZ, THE PRECHARGE TIME REQUIRED BY THE RAM DOES NOT MEET THE 95ns TIME AVAILABLE. (CLOCK FREQUENCIES OF 2·0 OR 2·5 MHZ ARE O.K.).

NOTE 2: THE TNRAS TIME REQUIRED BY THE RAM IS SATISFIED BY THE TNRAS TIME AVAILABLE AT ALL OF THE CLOCK FREQUENCIES CONSIDERED, (2·0, 2·5, AND 4·0 MHz).

NOTE 3: AT A CLOCK FREQUENCY OF 4·0 MHZ, THE TNRAS TIME REQUIRED BY THE RAM (250 NS) IS NOT SATISFIED BY TIME AVAILABLE (220 NS). (CLOCK FREQUENCIES OF 2·0 OR 2·5 MHZ ARE OK.)

DRAWN: D.M.P. 21-7-80

GREENBANK ELECTRONICS

MZB-3 REFRESH CYCLE TIMING

DRG. NO. 101873 | 1 OF 1

8.3.6.1 The diagram illustrates the main essentials of the CPU refresh cycle. As NMREQ is used directly to generate the row address strobe NRAS, the time for which this is low ('TR' on the diagram) is of importance.

8.3.6.2 For CPU clock frequencies of 2.0, 2.5, and 4.0 MHz, this parameter (TR) is 460ns, 360ns, and 220ns, respectively. The NRAS required is required by the 4116-4, and is 250ns for this device, and so it is unsuitable. (The 4116-4 will already have been eliminated for 4.0 MHz operation on the grounds of inadequate access time, so it will not matter that it must be eliminated again here.)

8.3.7 The Precharge times ('TP') for the three frequencies are 210ns, 160ns and 95ns. It will be seen that the worst device (4116-4) can easily be used at 2.0 MHz, and possibly 2.5 MHz, since 150ns for the 4116-4 is less than the 210ns and 160ns limits, but the 95ns available at 4.0 MHz is inadequate for any of the 4116s, even the fastest.

8.3.8 To summarise, the clock frequency of 2.0 MHz is ideal for static 450ns memories (e.g. 2708,2516,2114) and for the cheapest 4116-4 250ns dynamic RAMs, but a CPU clock frequency of 4.0 MHz requires WAIT states to be added for all but the very fastest of the static memories, and prohibits entirely the use of all the dynamic memories listed. (But remember some people neither know nor care about these detailed design points, and enjoy perfectly satisfactory operation with a 4.0 MHz CPU clock.)

8.3.9 Adding WAIT states cannot help the dynamic RAM precharge problem, since WAIT states cannot be inserted in the CPU refresh cycle. (Note, this is a defect in the Z80 CPU chip itself, not a defect in the MZB-3 board!)

8.3.10 There are methods of extending the precharge time and so permitting the use of dynamic RAMs with a 4.0 MHz clock, but the usual solutions involve the use of high speed 'Schottky' flip-flops, and the '$\overline{M1}$' signal, which is not an allocation on the ISBUS standard.

8.3.11 Therefore, based on the assumption that the user is reading these notes simply to get his MZB-3 board going, the following two solutions to the problems raised are offered:

(i) Ignore the precharge problem, and take a chance with the fastest 4116 you can obtain. The 4116-2 needs 100ns precharge and the cpu at 4.0 MHz offers 95ns so in fact there is every chance that a typical 4116-2 will not notice the missing 5ns, which after all is an exceedingly small time. (Even something travelling at the speed of light couldn't cover a couple of metres in 5ns!)

(ii) Make a modification, as described in Section 6.4 below so that clock frequencies of both 2.0 MHz and 4.0 MHz are readily available. In this way 2.0 MHz can be used while the system is being tested, and 4.0 MHz can be used for experimentation.

8.4 Modification to permit 2.0 MHz/4.0 MHz operation.

8.4.1 IC15b ($\frac{1}{2}$ D flip-flop) serves no useful purpose in the circuit as it stands, and it may be released to act as a divide-by-two counter to divide the 4.0 MHz clock down to a 2.0 MHz signal. Either of these frequencies can then be selected as the CPU clock.

8.4.2 The modified circuit is shown on drawing 101874 'MZB-3 Downgrade from 4.0 MHz to 2.0 MHz', on page 31, and the following step-by-step instructions should be read in conjunction with the information on the drawing.

8.4.3 Isolate pin 10 of IC15b by cutting tracks.

8.4.4 Reconnect IC15a to IC16 pin 4, and thus restore the circuit to virtually its original state.

8.4.5 Isolate IC9 pin 4.

8.4.6 Connect IC9 pin 4 to IC15b pin 11.

8.4.7 Connect IC15b pin 8 to IC15b pin 12.

8.4.8 Connect IC15b pin 10 and IC15b pin 13 to +5V (e.g. IC15b pin 14). It is not necessary to use a resistor in series to make the +5V connection for the reasons given at the foot of page 16.

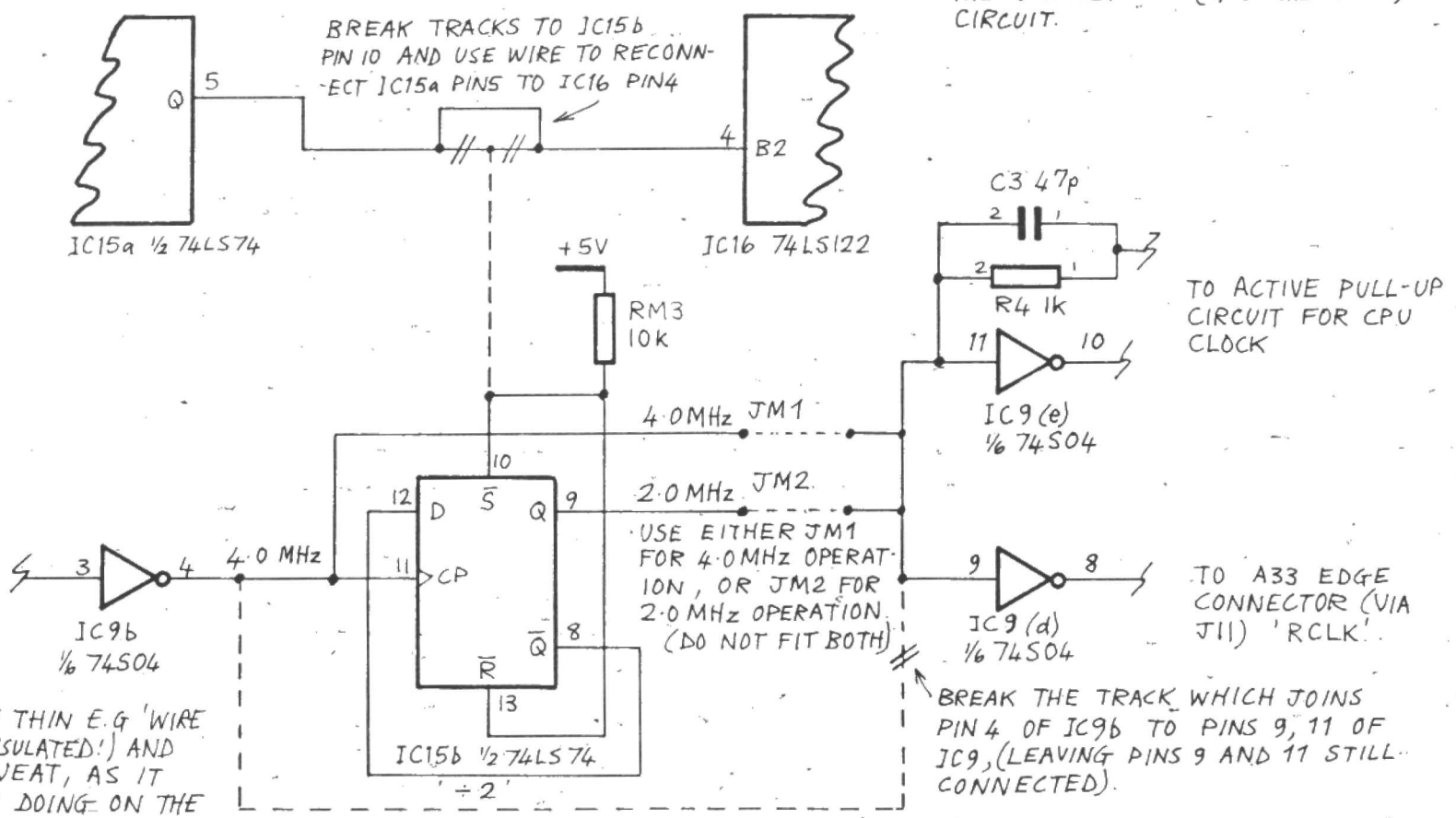
8.4.9 Connect IC9 pins 9,11 to IC9 pin 4 via jumper wire JM1 for 4.0 MHz operation as before.

8.4.10 Alternatively connect IC9 pins 9,11 to IC15b pin 9, via jumper wire JM2 for operation at 2.0 MHz.

8.4.11 The changeover from 4.0 MHz to 2.0 MHz may be by means of a switch if desired, but note this switch must not be operated whilst the CPU is running as data may be corrupted during the changeover. If, during the changeover, the CPU is stopped so effectively that M1 cycles cease, then it will prove impossible to restart the CPU without switching the system off. (This is because the Reset Circuit(Drg. No. 101810 sheet 2 page 34) needs the $\overline{ZM1}$ input on pin 9 of IC14c to let it produce the clock, pin 3 of IC15a: no clock = no reset!) At switch-on the R8-C5 combination provides another reset, regardless of the presence or absence of $\overline{ZM1}$.

DRG. Nº 101874 | 1 OF 1

SEE DRAWING NO. 101810 SHEETS 1 AND 2 FOR THE DIAGRAM OF THE UNMODIFIED (4·0 MHz ONLY) CIRCUIT.



NOTE: USE VERY THIN E.G 'WIRE WRAP' WIRE (INSULATED!) AND KEEP WIRING NEAT, AS IT MOSTLY NEEDS DOING ON THE REVERSE; I.E. NON-COMPONENT SIDE OF THE BOARD, UNLESS IT IS PASSED THROUGH THE SAME HOLES AS THE IC SOCKET PINS.

MODIFICATION TO HALVE THE CPU CLOCK FREQUENCY AND SO PERMIT 450 nS MEMORIES (e.g IC11, 2516) TO BE USED WITHOUT WAIT STATES, AND TO HELP INTERFACE RESTRICTIONS ON DYNAMIC RAM BOARD MXD-2.

	MOD 002 DMP 4·8·80	DRAWN: D.M.P 21-7-80	GREENBANK ELECTRONICS
			MZ80-3 DOWNGRADE FROM 4 MHz TO 2 MHz
			DRG. NO. 101874 | 1 OF 1

9. Appendix 2: Use of 6.0 MHz CPU Clock Frequency

9.1 During the manufacture of the Z80/MK3880 CPU chip, the devices made are divided into at least 3 categories: 4.0 MHz, 2.5 MHz, and fail. (The classifications are made on the basis of actual performance measurements on the chips, which explains why it is so rare to find one which is defective - they all have to be tested before they are numbered, to see what number is required!)

9.2 As more and more improvements are made in the manufacturing process, more and more of the devices manufactured fall into the highest category, with the result that there is only a small price difference at the moment between 2.5 MHz and 4.0 MHz CPU chips of the Z80 type.

9.3 An example of such an improvement is the actual reduction in size of the CPU chip itself, which makes it run faster, other things being equal. It is likely that so many of the present 4.0 MHz chips will be capable of running at frequencies vastly in excess of 4.0 MHz, that it will be worth the manufacturers' whiles to introduce a new category and charge a premium for this. It appears that the new category will be a 6.0 MHz type.

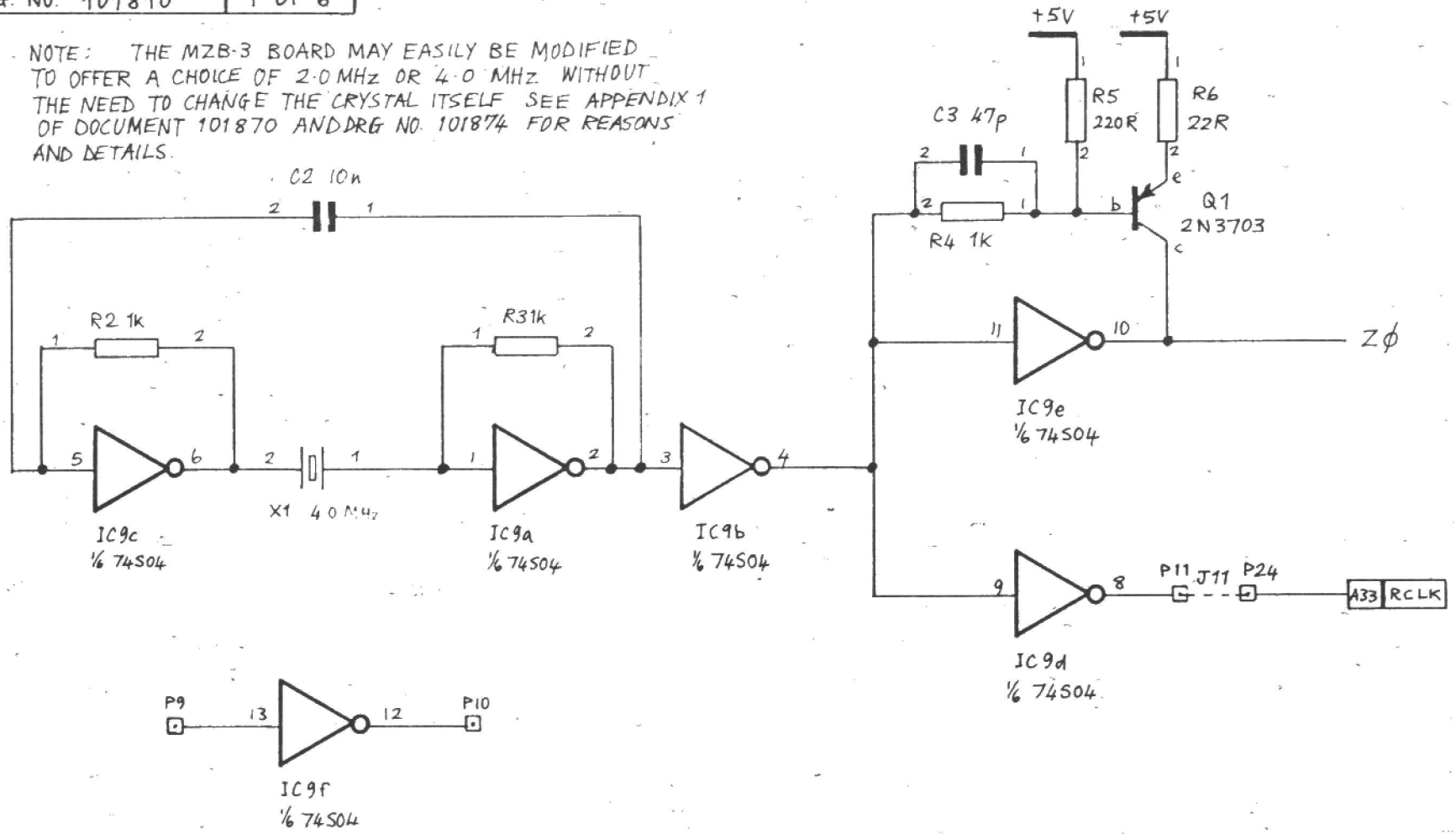
9.4 Our own recommendation, which of course must necessarily be individual to us, is that the 6.0 MHz CPU frquency will be difficult to use effectively until the performance of the memory components which are generally (i.e. cheaply) available, is similarly improved.

9.5 For example, the point raised in section 8.3.7, regarding the precharge time for dynamic RAMs is even more important at 6.0 MHz. It is possible to extend the precharge time with a 4.0 MHz clock, as indicated in section 8.3.10, but it is likely that this will not be so easy at 6.0 MHz.

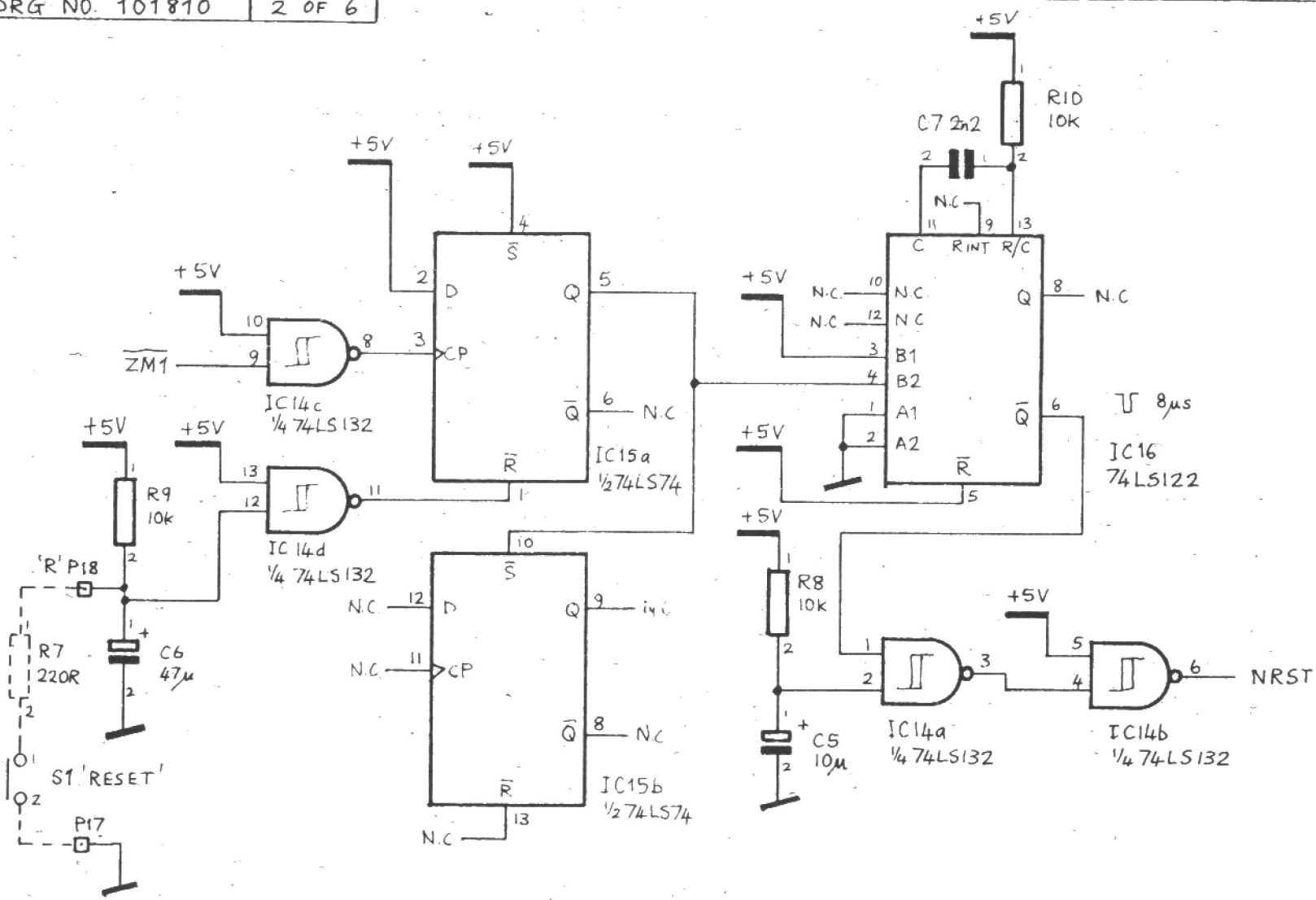
9.6 At the time of writing 6.0 MHz CPU chips are not generally available, although probably a lot of 4.0 MHz CPUs will operate at 6.0 MHz, and there is no detailed data which can be used to start to solve such problems as the dynamic RAM precharge time extension.

DRG. NO. 101810 | 1 OF 6

NOTE: THE MZB-3 BOARD MAY EASILY BE MODIFIED TO OFFER A CHOICE OF 2·0 MHz OR 4·0 MHz WITHOUT THE NEED TO CHANGE THE CRYSTAL ITSELF SEE APPENDIX 1 OF DOCUMENT 101870 AND DRG NO. 101874 FOR REASONS AND DETAILS.



		ISSUE 1 : 15. 7. 80	DRAWN : D.M.P. 15.7.80	GREENBANK ELECTRONICS
				MZB-3 CIRCUIT DIAGRAM (CLOCK OSCILLATOR)
				DRG. NO. 101810 | 1 OF 6



	ISSUE 1 15.7.80	DRAWN: DMP 15.7.80	GREENBANK ELECTRONICS
			MZB-3 CIRCUIT DIAGRAM (RESET CIRCUITRY)
			DRG. NO 101810 | 2 OF 6

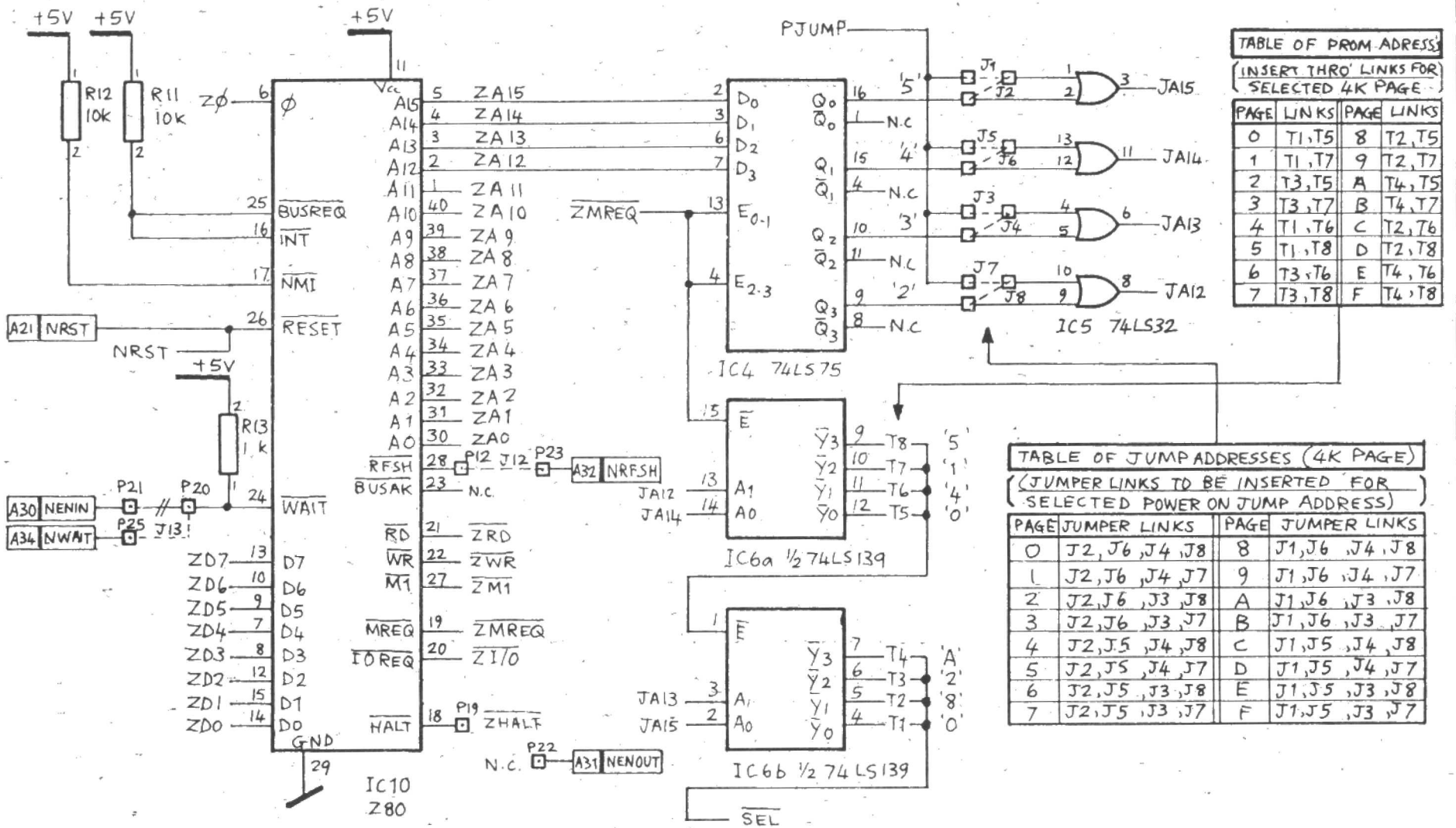


TABLE OF PROM ADRESS
(INSERT THRO' LINKS FOR SELECTED 4K PAGE)

PAGE	LINKS	PAGE	LINKS
0	T1,T5	8	T2,T5
1	T1,T7	9	T2,T7
2	T3,T5	A	T4,T5
3	T3,T7	B	T4,T7
4	T1,T6	C	T2,T6
5	T1,T8	D	T2,T8
6	T3,T6	E	T4,T6
7	T3,T8	F	T4,T8

TABLE OF JUMP ADDRESSES (4K PAGE)
(JUMPER LINKS TO BE INSERTED FOR SELECTED POWER ON JUMP ADDRESS)

PAGE	JUMPER LINKS	PAGE	JUMPER LINKS
0	J2,J6,J4,J8	8	J1,J6,J4,J8
1	J2,J6,J4,J7	9	J1,J6,J4,J7
2	J2,J6,J3,J8	A	J1,J6,J3,J8
3	J2,J6,J3,J7	B	J1,J6,J3,J7
4	J2,J5,J4,J8	C	J1,J5,J4,J8
5	J2,J5,J4,J7	D	J1,J5,J4,J7
6	J2,J5,J3,J8	E	J1,J5,J3,J8
7	J2,J5,J3,J7	F	J1,J5,J3,J7

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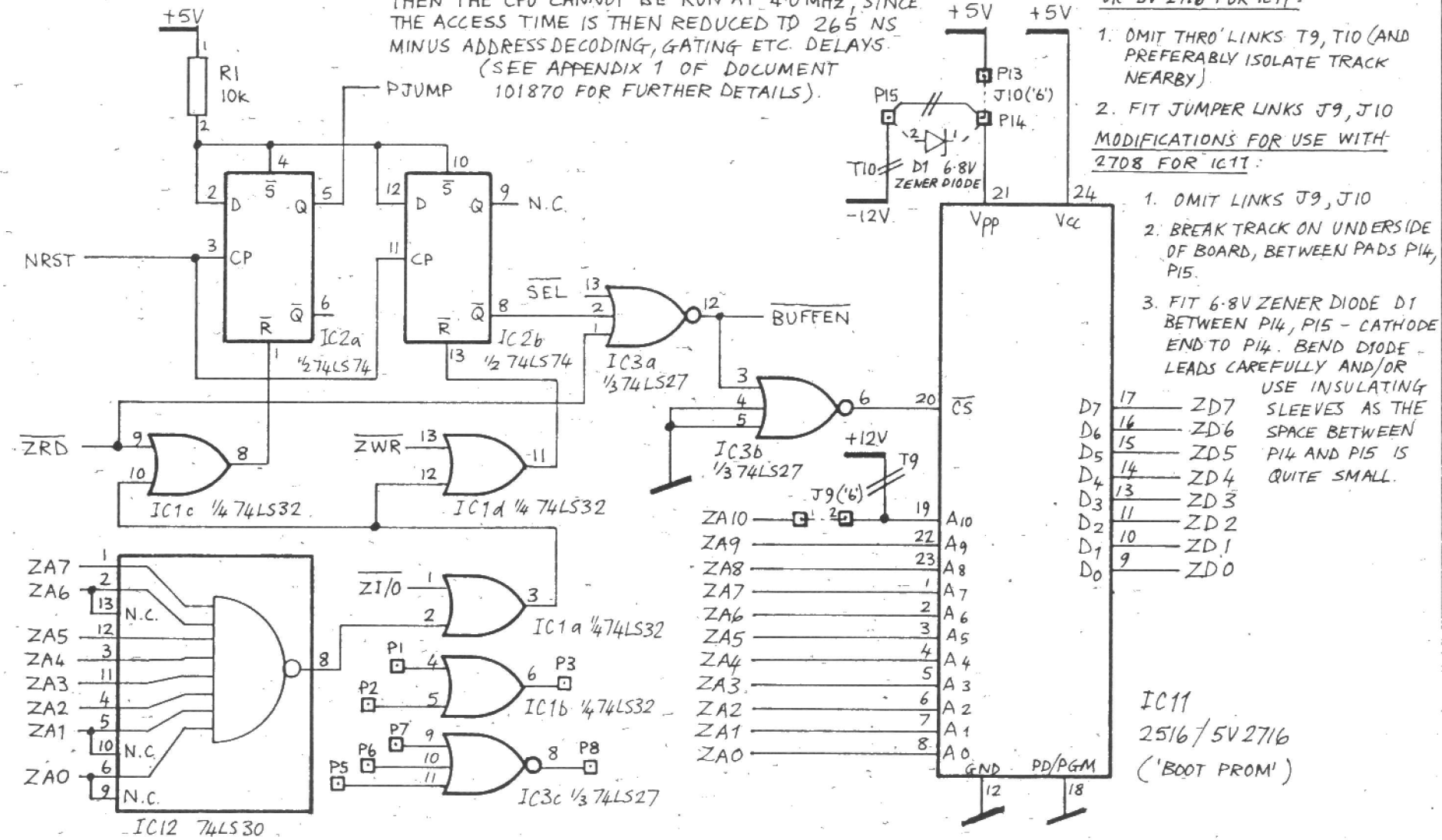
GREENBANK ELECTRONICS

MZB-3 CIRCUIT DIAGRAM
(CPU AND POWER ON JUMP)

DRG NO. 101810 | 3 OF 6

NOTE: IF IC11 IS A STANDARD 450 NS COMPONENT THEN THE CPU CANNOT BE RUN AT 4·0 MHz, SINCE THE ACCESS TIME IS THEN REDUCED TO 265 NS MINUS ADDRESS DECODING, GATING ETC. DELAYS. (SEE APPENDIX 1 OF DOCUMENT 101870 FOR FURTHER DETAILS).



SHOWN WIRED FOR USE WITH 2516 OR 5V 2716 FOR IC11 :

1. OMIT THRO' LINKS T9, T10 (AND PREFERABLY ISOLATE TRACK NEARBY)
2. FIT JUMPER LINKS J9, J10

MODIFICATIONS FOR USE WITH 2708 FOR IC11 :

1. OMIT LINKS J9, J10
2. BREAK TRACK ON UNDERSIDE OF BOARD, BETWEEN PADS P14, P15.
3. FIT 6·8V ZENER DIODE D1 BETWEEN P14, P15 – CATHODE END TO P14. BEND DIODE LEADS CAREFULLY AND/OR USE INSULATING SLEEVES AS THE SPACE BETWEEN P14 AND P15 IS QUITE SMALL.

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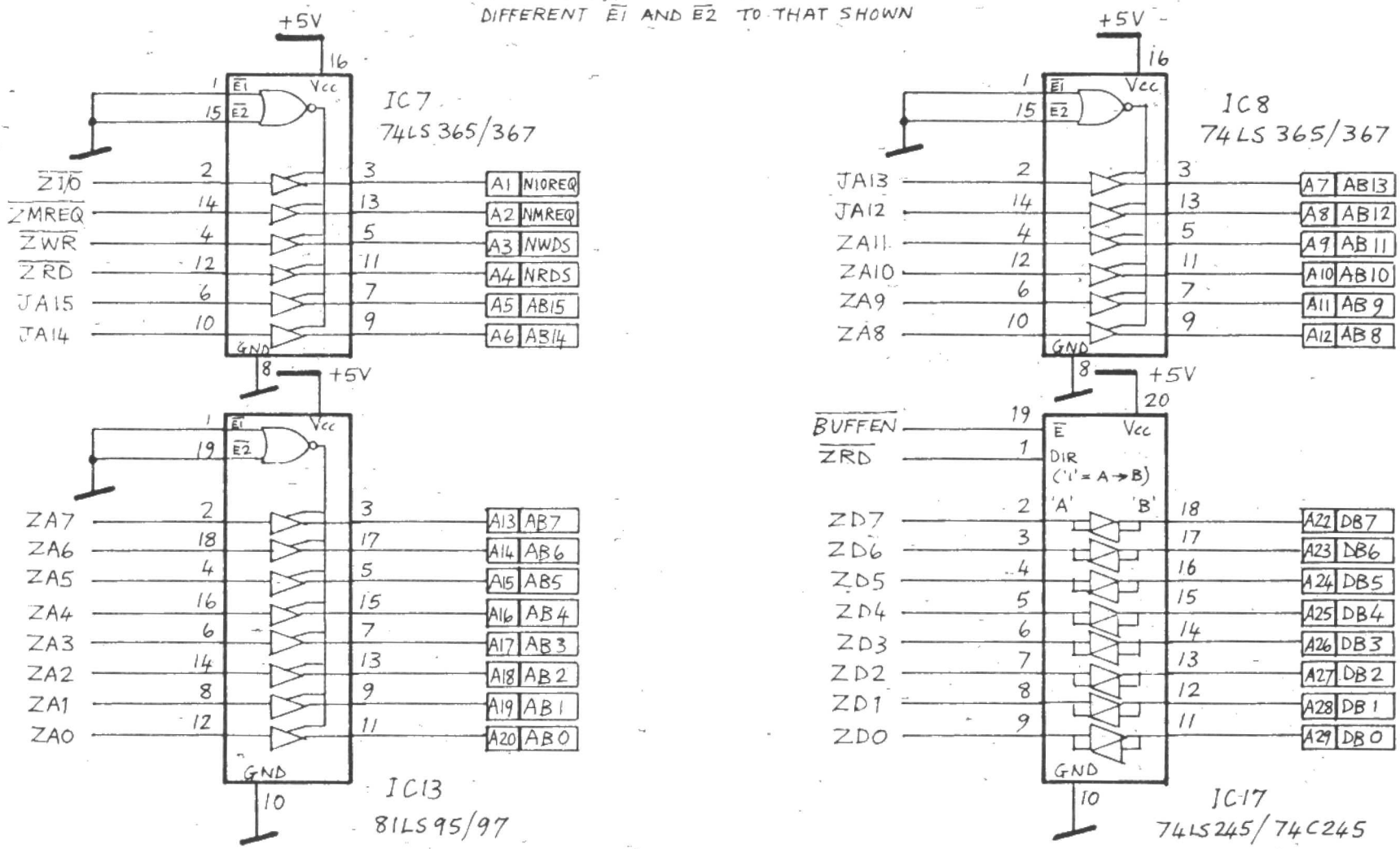
		MZB-3 CIRCUIT DIAGRAM (BOOT PROM AND CONTROLLER)	
		DRG. NO. 101810	4 OF 6

NOTE: IC7, IC8 : 74LS367 HAS SLIGHTLY DIFFERENT $\overline{E1}$ AND $\overline{E2}$ TO THAT SHOWN



NOTE: IC13: 81LS97 HAS SLIGHTLY DIFFERENT $\overline{E_1}$ AND $\overline{E2}$ TO THAT SHOWN

		ISSUE 1: 15.7.80	DRAWN: D.M.P. 15.7.80	GREENBANK ELECTRONICS
				MZB-3 CIRCUIT DIAGRAM (ADDRESS, DATA, AND CONTROL BUS BUFFERS)
				DRG. NO. 101810 | 5 OF 6

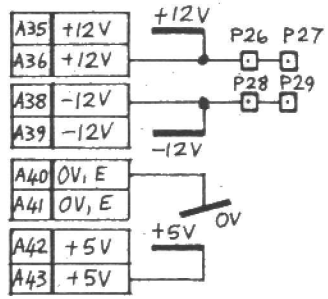
POWER SUPPLY PIN DATA FOR INTEGRATED CIRCUITS USED

REF.	TYPE	-5V	0V	+5V	+12V
IC1	74LS32	-	7	14	-
IC2	74LS74	-	7	14	-
IC3	74LS27	-	7	14	-
IC4	74LS75	-	12	5	-
IC5	74LS32	-	7	14	-
IC6	74LS139	-	8	16	-
IC7	74LS365/ 74LS367	-	8	16	-
IC8	74LS365/ 74LS367	-	8	16	-
IC9	74S04	-	7	14	-
IC10	Z80A/ MK3880N	-	29	11	-
IC11	2516/ 2716(5V)	-	12	24, 21	-
-OR-	(2708)	(21)	(12)	(24)	(19)
IC12	74LS30	-	7	14	-
IC13	81LS95/ 81LS97	-	10	20	-
IC14	74LS132	-	7	14	-
IC15	74LS74	-	7	14	-
IC16	74LS122	-	7	14	-
IC17	74LS245/ 74C245	-	10	20	-

(THERE ARE NO GOLD FINGERS PROVIDED ON THE WHOLE OF THE 'B' SIDE - B1 – B43)

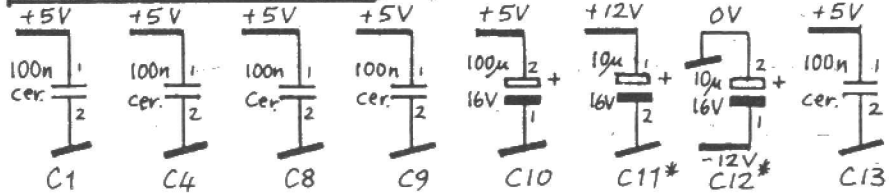
POLARISING SLOT (IF USED) SHOULD BE POSITIONS A37, B37

POWER SUPPLIES



CONNECTIONS TO THE POWER RAILS FOR OTHER PURPOSES e.g. 'ENABLES' OR 'DISABLES' ETC., ARE SHOWN ON THE MAIN CIRCUIT DIAGRAMS.

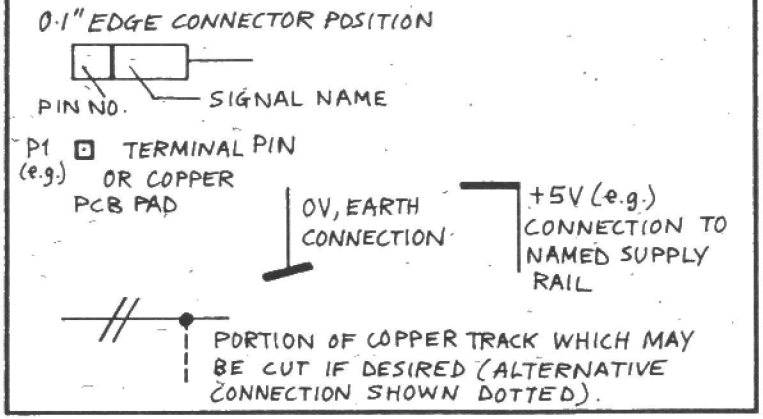
DECOUPLING CAPACITORS



* C11, C12 ARE NOT REQUIRED UNLESS IC11 IS A TYPE 2708.

KEY TO SYMBOLS USED ON CIRCUIT DIAGRAMS.

(SIGNAL NAMES WHICH ARE NOT IDENTIFIED IN THE MANNER BELOW ARE FOR REFERENCE ONLY).



		ISSUE 1 : 15-7-80	DRAWN: D.M.P. 15.7.80

GREENBANK ELECTRONICS

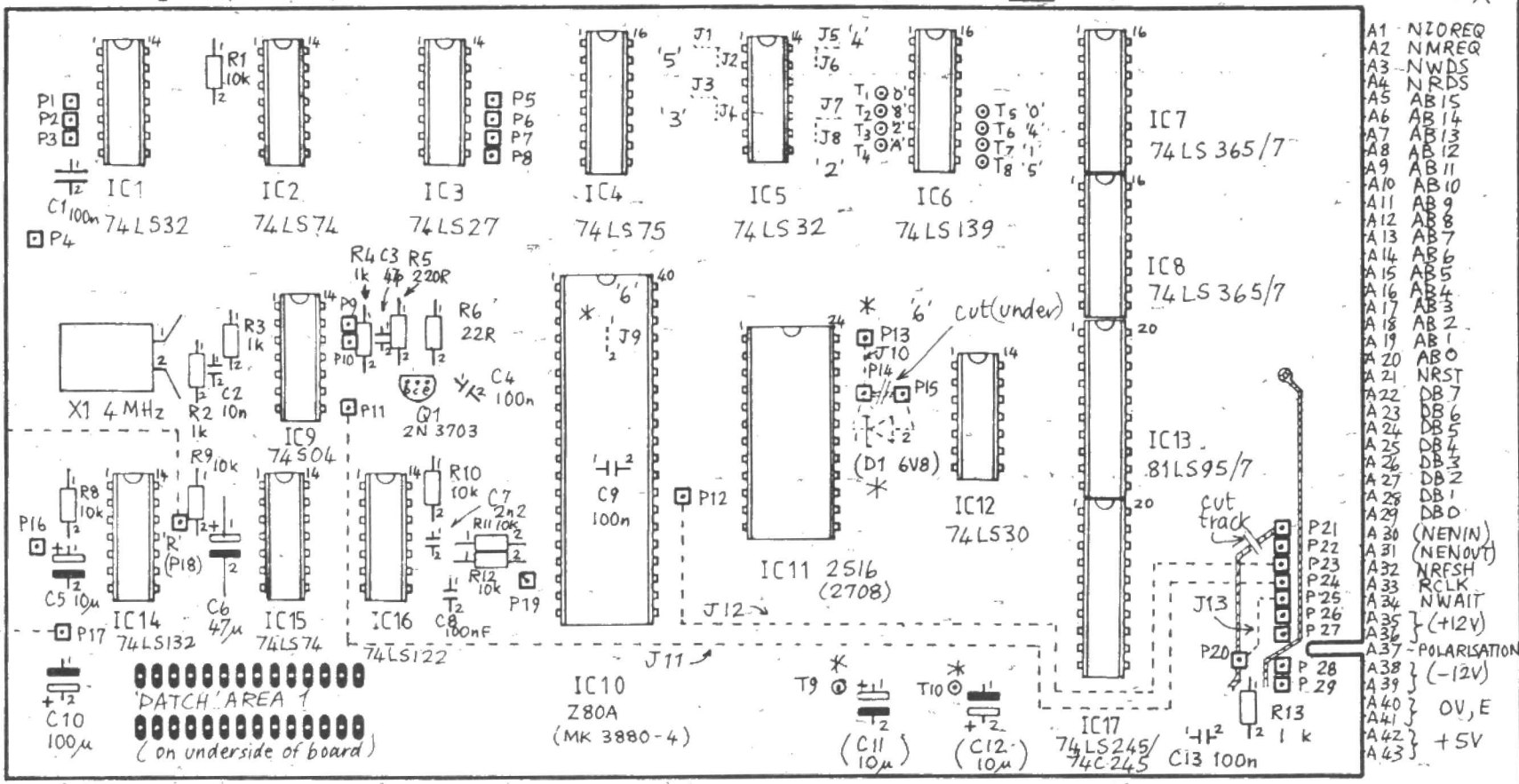
MZB-3 CIRCUIT DIAGRAM (POWER SUPPLIES AND GENERAL INFORM-ATION)

DRG. NO. 101810 | 6 OF 6

DRG NO. 101830	1 OF 1

J1,3 end 1, J5,7 end 2 ↖

Note: The following components, if fitted, will need one end soldering to the top side of the board: D1 end 2, ↗



NOTE:
THERE ARE NUMEROUS WIRE THROUGH LINKS WHICH ARE NOT SHOWN ABOVE, BUT WHICH MUST BE FITTED. (DO NOT FIT ANY OF THE NUMBERED THROUGH LINKS T1 - T10 OR JUMPERS J1 TO J10 UNTIL YOU UNDERSTAND THEIR PURPOSE - SEE TABLES ON DRG. NO. 101810 SHEETS 3 AND 4).

* IMPORTANT: THERE ARE CHANGES IN THESE AREAS, ACCORDING TO WHETHER IC11 IS TYPE 2516 OR 2708 - SEE NOTES ON SHEET 4 OF CIRCUIT DIAGRAM (DRG. NO. 101810) FOR GUIDANCE

OMIT C9 IF IT WILL NOT FIT.	EVEN IF YOU ARE NOT USING J13 TO CONNECT THE NWAIT LINE SOLDER BOTH SIDES OF P20.	ISSUE 1: 23-7-80 MOD 002: D.M.P. 4-8-80	DRAWN: D.M.P. 15-7-80	GREENBANK ELECTRONICS MZB-3 ASSEMBLY DRAWING DRG. NO. 101830 | 1 OF 1

COMPONENT PARTS LIST FOR MZB-3 Document Ref: 101840

Issue: 3 Date: 22.7.80 , 4.8.80, 21.5.81

LISTED BY COMPONENT REFERENCE NO.

Resistors ¼W

R1	10k	R8	10k
R2	1k	R9	10k
R3	1k	R10	10k
R4	1k	R11	10k
R5	220R	R12	10k
R6	22R	R13	1k
R7	220R		

Capacitors

C1	100n	C8	100n
C2	10n	C9	100n
C3	47p	C10	100u/16V
C4	100n	(C11)	(10u/16V)
C5	10u/16V	(C12)	(10u/16V)
C7	2n2		

Diode (D1) (6.8V Zener)

Transistor Q1 2N3703

Quartz Xtal X1 4.0 MHz

Integrated Circuits (use sockets)

IC1	74LS32	IC10	Z80A/MK3880-4
IC2	74LS74	(IC11)	(2516)
IC3	74LS27	IC12	74LS30
IC4	74LS75	IC13	81LS95/97
IC5	74LS32	IC14	74LS132
IC6	74LS139	IC15	74LS74
IC7	74LS365/7	IC16	74LS74
IC8	74LS365/7	IC17	74LS245/ 74C245
IC9	74S04		

Reset Switch

S1 1 Type SW9 Min Push

LISTED BY COMPONENT VALUE

Resistors ¼W

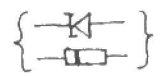
22R	1	R6	Red,red,black
220R	2	R5,7	Red,red,brown
1k		R2,3,4	Brown,black,red
10k		R1,8-13	Brown,black, orange

Capacitors

47p	1	C3	
2n2	1	C7	
10n	1	C2	
100n	5	C1,4,8,9,13	
10u/16V	1(3)	C5,(11),(12)	
47u/10V	1	C6	
100u/16V	1	C10	

Diode

6.8V Zener (1) (D1)



Transistor

2N3703 1 Q1

Quartz 4.0 MHz 1 X1

Integrated Circuits (use sockets)

74LS27	(14 pin)	1	IC3
74LS30	(14 ")	1	IC12
74LS32	(14 ")	2	IC1,5
74LS74	(14 ")	2	IC2,15
74LS75	(16 ")	1	IC4
74LS122	(14 ")	1	IC16
74LS132	(14 ")	1	IC14
74LS139	(16 ")	1	IC6
74LS245/74C245	(20 pin)	1	IC17
74LS365/LS367	(16 ")	2	IC7,8
74S04	(14 pin)	1	IC9
81LS95/81LS97	(20 pin)	1	IC13
Z80A/MK3880-4	(40 ")	1	IC10
2516	(24 ")	1	IC11

Switch. Min. Push type SW9 S1

Sockets for ICs

14 pin	9	IC1-3,5,9,12,14-16
16 "	4	IC4,6,7,8
20 "	2	IC13,17
24 "	1	IC11
40 "	1	IC10

Note: D1, C11, C12 are only required if a type 2708 (multi-rail) is used for IC11; the newer type 2516 has twice the memory capacity and needs only a single 5V supply rail.